Specification for Approval

PRODUCT NAME: **RGC15128128FH039**
PRODUCT NO.:   **9923905000**

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2011. 02. 18	
A01	■ Transfer from X version ■ Add the information of module weight ■ Add the packing specification	2011. 04. 20	Page 5 & 17

CONTENTS

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http://www.ritdisplay.com

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : 262K color and 65K colors
- Panel matrix : 128*128
- Driver IC : SSD1351
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.41mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C.
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x (RxGxB) x 128 (H)	dot
2	Dot Size	0.0435 (W) x 0.1855 (H)	mm^2
3	Dot Pitch	0.0685 (W) x 0.2055 (H)	mm^2
4	Aperture Rate	57	%
5	Active Area	26.279 (W) x 26.284 (H)	mm^2
6	Panel Size	33.5 (W) x 33.5 (H)	mm^2
7*	Panel Thickness	1.22 ± 0.1	mm
8	Module Size	33.5 (W) x 57.17 (H) x 1.41 (D)	mm^3
9	Diagonal A/A size	1.46	inch
10	Module Weight	3.46 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue
  thickness.

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5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	4	V	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	10	19	V	Ta = 25°C	IC maximum rating
Supply Voltage (V_{DDIO})	-0.5	V_{CI}	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity	-	85	%		
Life Time	11,000	-	Hrs	90 cd/m^2, 50% checkerboard	Note (1)
Life Time	14,000	-	Hrs	70 cd/m^2, 50% checkerboard	Note (2)

Note:

   (A) Under Vcc = 16.5V, Ta = 25°C, 50% RH.

   (B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 90 cd/m^2 :

- Master contrast setting : 0x0b
- Red contrast setting : 0x70
- Green contrast setting : 0x71
- Blue contrast setting : 0x94
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Setting of 70 cd/m^2 :

- Master contrast setting : 0x09
- Red contrast setting : 0x66
- Green contrast setting : 0x6a
- Blue contrast setting : 0x89
- Frame rate : 105Hz
- Duty setting : 1/128

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6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)		16	16.5	17	V
V_{CI}	Digital power supply		2.4	-	3.5	V
V_{DDIO}	I/O voltage power supply		1.65	-	V_{CI}	V
I_{DD}	$V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16V$, External $V_{DD} = 2.6V$, Display ON, No panel attached, contrast = FF			170	190	uA
I_{DDIO}	$V_{CI} = V_{DDIO} =$, 3.5V, $V_{CC} = 16V$, Display ON, No panel attached, contrast = FF	External VDD = 2.6V		0.5	10	uA
		Internal VDD		0.5	10	uA
I_{CI}	$V_{CI} = V_{DDIO} =$, 3.5V, $V_{CC} = 16V$, Display ON, No panel attached, contrast = FF	External VDD = 2.6V	-	60	70	uA
		Internal VDD		255	280	uA
I_{CC}	$V_{CI} = V_{DDIO} =$, 3.5V, $V_{CC} = 16V$, Display ON, No panel attached, contrast = FF	External VDD = 2.6V	-	1.15	1.26	mA
		Internal VDD		1.15	1.26	mA
V_{IH}	Hi logic input level		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low logic input level		0	-	0.2* V_{DDIO}	V
V_{OH}	Hi logic output level		0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low logic output level		0	-	0.1* V_{DDIO}	V
I_{SEG}	Segment Output Current Setting $V_{CC} = 16V$ at IREF = 12.5uA	Contrast=FF	-	200	-	uA
		Contrast=7F	-	100	-	uA
		Contrast=3F	-	50	-	uA

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6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

| PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		30	32	mA	All pixels on (1)
Standby mode current		3	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		495	528	mW	All pixels on (1)
Standby mode power consumption		49.5	66	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	70	90		cd/m^2	Display Average
Standby mode Luminance		20		cd/m^2	
CIEx (White)	0.24	0.28	0.32		
CIEy (White)	0.28	0.32	0.36		
CIEx (Red)	0.62	0.66	0.70		
CIEy (Red)	0.29	0.33	0.37		
CIEx (Green)	0.26	0.30	0.34		x, y (CIE 1931)
CIEy (Green)	0.59	0.63	0.67		
CIEx (Blue)	0.10	0.14	0.18		
CIEy (Blue)	0.14	0.18	0.22		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		µs	

(1) Normal mode condition :

- Driving Voltage : 16.5V

- Master contrast setting : 0x0b

- Red contrast setting : 0x70

- Green contrast setting : 0x71

- Blue contrast setting : 0x94

- Frame rate : 105Hz
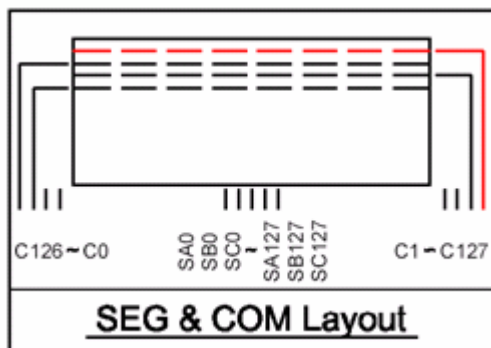
- Duty setting : 1/128

(2) Standby mode condition :

- Driving Voltage : 16.5V

- Master contrast setting : 0x04

- Red contrast setting : 0x4e

- Green contrast setting : 0x53

- Blue contrast setting : 0x6e

- Frame rate : 105Hz

- Duty setting : 1/128

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM
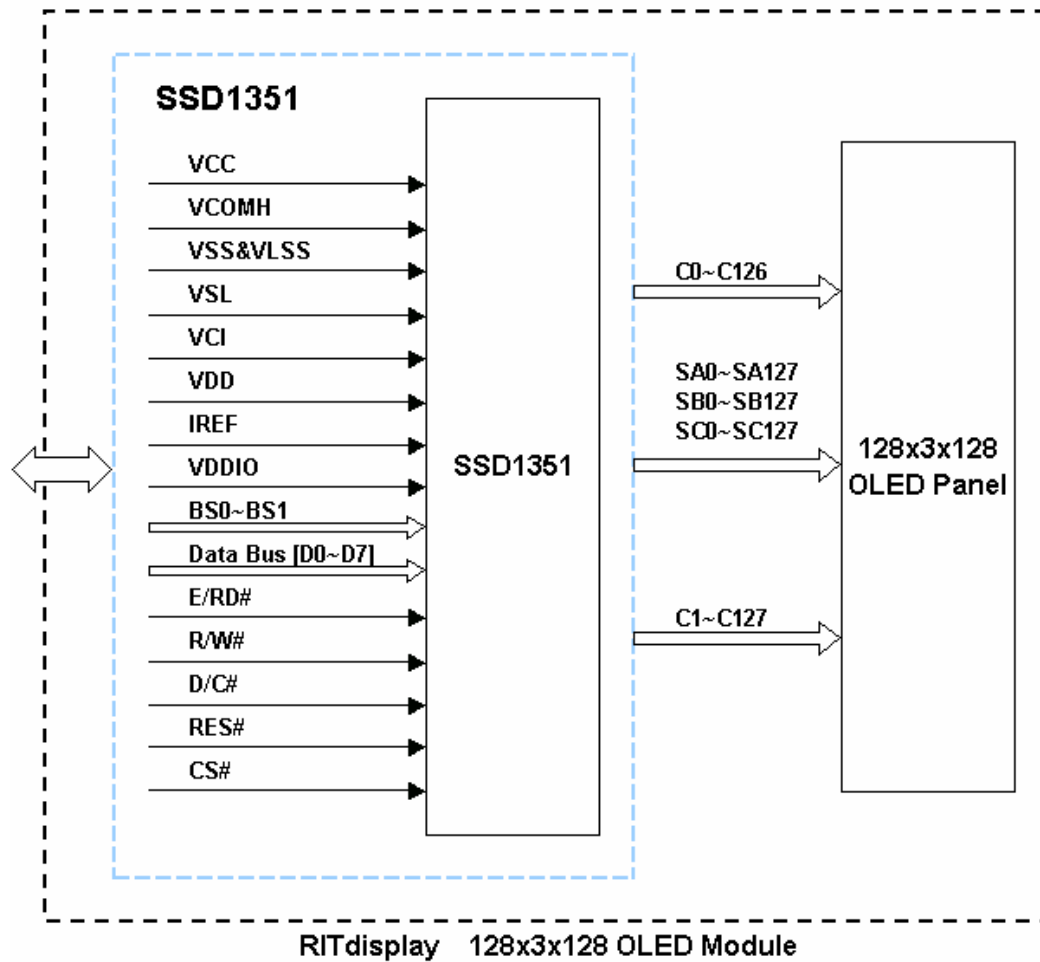
7.2 PANEL LAYOUT DIAGRAM

7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	RES#	Hardware Reset pin (Low active).
2	IREF	A resistor should be connected between this pin and VSS.
3	D/C#	H: Data, L: Command.
4	VDD	Power supply pin for core logic operation.
5	CS#	Chip select pin.
6	VCI	Digital voltage power supply.
7	BS1	Interface select pin. (8080: BS1=1)
8	VCC	Power supply for panel driving voltage.
9	BS0	Interface select pin. (8080: BS0=0)
10	VLSS	Analog system ground pin
11	R/W#	8080: data write enable pin; 6800:Read/Write select pin.
12	NC	No connection.
13	E/RD#	8080: data read enable pin; 6800:Read/Write enable pin.
14	NC	No connection.
15	D0	This pin is data pin.
16	NC	No connection.
17	D1	This pin is data pin.
18	NC	No connection.
19	D2	This pin is data pin.
20	NC	No connection.
21	D3	This pin is data pin.
22	VSS	Ground.
23	D4	This pin is data pin.
24	VCC	Power supply for panel driving voltage.
25	D5	This pin is data pin.
26	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin an VSS.
27	D6	This pin is data pin.
28	VDDIO	Power supply for interface logic level.
29	D7	This pin is data pin.
30	VSL	This is segment voltage reference pin.

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7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 128 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

| Segment Address	Normal	0			1			2	......	......	126	127			
	Remapped	127			126			125	......	......	1	0			
Color		A	B	C	A	B	C	A			C	A	B	C	
Data Format		A5	B5	C5	A5	B5	C5	A5	......	......	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	......	......	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	......	......	C3	A3	B3	C3	
Common Address		A2	B2	C2	A2	B2	C2	A2	......	......	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	......	......	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	......	......	C0	A0	B0	C0	
Normal	Remapped														Common output
0	127	6	6	6	6	6	6	6	......	......	6	6	6	6	COM0
1	126	6	6	6	6	6	6	6	......	......	6	6	6	6	COM1
2	125	6	6	6	6	6	6	6	......	......	6	6	6	6	COM2
3	124	6	6	6	6	6	6	6	......	......	6	6	6	6	COM3
4	123	6	6	6	6	6	6	6	......	......	6	6	6	6	COM4
5	122	6	6	6	6	6	6	6	......	......	6	6	6	6	COM5
6	121	6	6	no of bits in this cell			6	6	......	......	6	6	6	6	COM6
7	120								......	......	6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	......	......	:	:	:	:	:
:	:	:	:	:	:	:	:	:	......	......	:	:	:	:	:
:	:	:	:	:	:	:	:	:	......	......	:	:	:	:	:
123	4	6	6	6	6	6	6	6	......	......	6	6	6	6	:
124	3	6	6	6	6	6	6	6	......	......	6	6	6	6	COM124
125	2	6	6	6	6	6	6	6	......	......	6	6	6	6	COM125
126	1	6	6	6	6	6	6	6	......	......	6	6	6	6	COM126
127	0	6	6	6	6	6	6	6	......	......	6	6	6	6	COM127
SEG output		SA0	SB0	SC0	SA1	SB1	SC1	SA2	......	......	SC126	SA127	SB127	SC127	

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7.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	46	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle

Read cycle
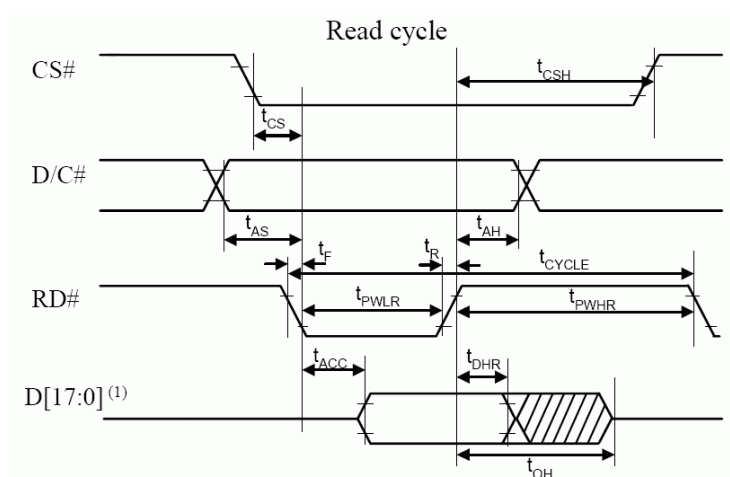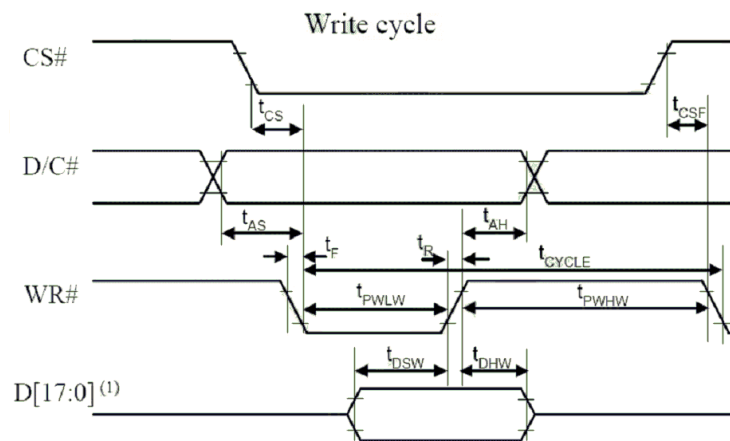
Note

(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

1. Power ON V_{CI}, V_{DDIO}.
2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

The Power ON sequence.
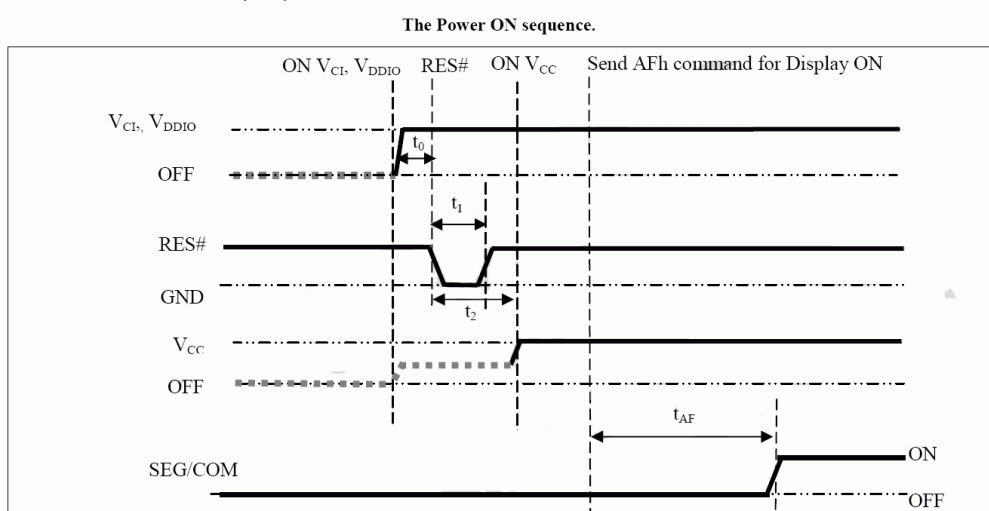
Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2]
3. Wait for t_{OFF}. Power OFF V_{CI}, V_{DDIO}.(where Minimum t_{OFF}=80ms [3], Typical t_{OFF}=100ms)

The Power OFF sequence
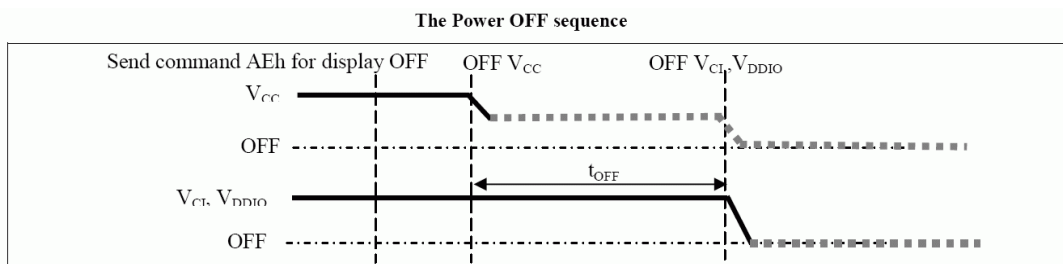
Note:

[1] Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
[2] V_{CC} should be kept float (disable) when it is OFF.
[3] V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.
[4] The register values are reset after t_1.
[5] Power pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

8.2 APPLICATION CIRCUIT
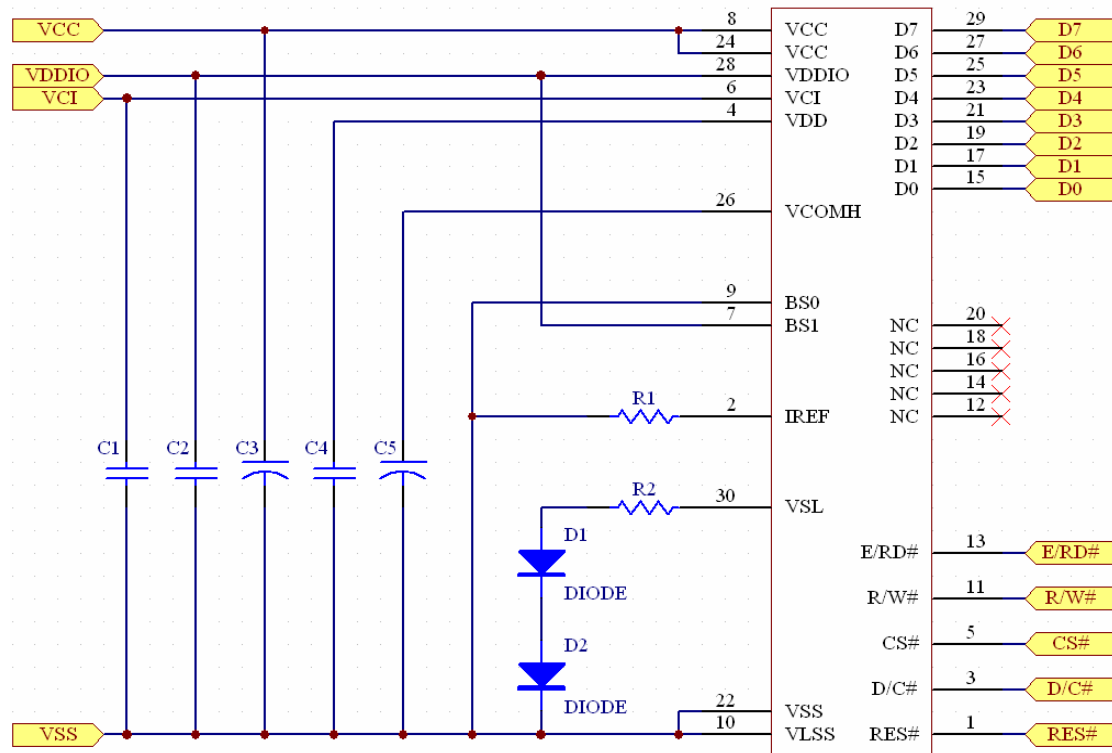
Recommend components：

C1, C2, C4: 1uF/16V(0805)

C3, C5: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 1M ohm 1%(0603)

R2: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 8-bit interface

8.3 COMMAND TABLE

Refer to SSD1351 IC Spec.

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10. EXTERNAL DIMENSION

Specification:
1. Display: OLED (Full)
2. Dot Matrix: 128x3x128
3. Dot Size: 0.0435x0.1855mm
4. Dot Pitch: 0.0685x0.2055mm
5. Aperture Rate: 57%
6. Active Area: 26.279x26.284mm
7. IC: SSD1351U4R1

Pin Assignment

NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL
1	RES#	11	NC	21	VSS
2	IREF	12	R/W#	22	D3
3	D/C#	13	E/RD#	23	D4
4	VDD	14	NC	24	VCC
5	CS#	15	D0	25	D5
6	VCI	16	NC	26	VCOMH
7	BS1	17	D1	27	D6
8	VCC	18	NC	28	VDDIO
9	BS0	19	D2	29	D7
10	VLSS	20	NC	30	VSL

PROJECT CODE: P23905

PART NAME	Module Ass'y	REVISION	03
PARTS NO.	9823905000	REVISION	03

	Scale	Unscale		Sheet	1/1
	Module	David Li	Spec.	Irene Fan	
			Approved	Strong Tsai	
	Unit	mm			

CONFIDENTIAL

M.E.	Valerie Lo	E.E.	Song Huang

General Tolerance

Length (mm)	Tolerance(mm)
0 ~ 8	±0.1
8 ~ 25	±0.2
25 ~ 50	±0.3

128x3x128 Dots (1.46")

Single Tape
TERAOKA 631S
27.5x12.5x0.05mm
(Tape on Back)

Panasonic:
BTB header
AXE630224

Handler
15x5x0.15mm

AG Polarizer
t=0.19mm

SEG & COM Layout

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11. PACKING SPECIFICATION

The packing specification drawing contains the following labeled components:

Items and descriptions:

Item	Part No.	Description	QTY
1	9823905000	P23905 Module Ass'y	960
2	3008000103	Tray 330x270x8.7mm, t=0.7mm	42
3	3010000003	5G Silica Gel Desiccants	8
4	3003000012	Vacuum Bag 480x285x90mm	2
5	3003000016	Antistatic Bubble Bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88 , B corrugated	2
7	3000000009	Carton , 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	Tape	3

Component annotations in drawing:

- ① P23905 Module P/N:9823905000 Face Up,rotate packing 面朝上 旋轉放置
- ② Packing Tray P/N:3008000103 330x270x8.7mm, t=0.7mm
- ③ 5G Silica Gel Desiccants P/N:3010000003 5G 矽膠乾燥劑 x4
- ④ Vacuum Bag ONY/LDPE 真空包裝袋 ONY/LDPE P/N:3003000012 480x285x90mm Vacuum Packing:4 sec 抽真空4秒
- ⑤ Antistatic Bubble Bag 抗靜電氣泡袋 P/N:3003000016 440x(350+450)mm
- ⑥ Pizza Box P/N:3001000005 345x285x88 , B corrugated B浪
- ⑦ Carton P/N:3000000009 385x305x203mm
- ⑧ Label 標籤 P/N:3006000000
- ⑨ Tape 封箱膠帶 P/N:3208000125

- x 1 pcs(empty)
- x 20 pcs
- Rotate stack 旋轉堆疊
- x 21 pcs
- x2 pcs
- x1 pcs
- Packing Tray Instruction

Revision	Date	Note
01	2010/12/01	Packing Tray Instruction

General Tolerance

Length (mm)	Tolerance(mm)
0 ~ 8	±0.1
8 ~ 25	±0.2
25 ~ 50	±0.3

CONFIDENTIAL	Scale	Unit	Sheet
	1:9	mm	1/1
Third Angle Projection	Module	Spec.	Approved
M.E.	E.E.		
Iven Lee	Kevan Huang	Irene Fan	Strong Tsai
		David Li	

PROJECT CODE: P23905
PART NAME: Packing Tray Instruction REVISION 01
PARTS NO.: 9923905000 REVISION 01

RITEK GROUP RiTdisplay Corporation

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12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.
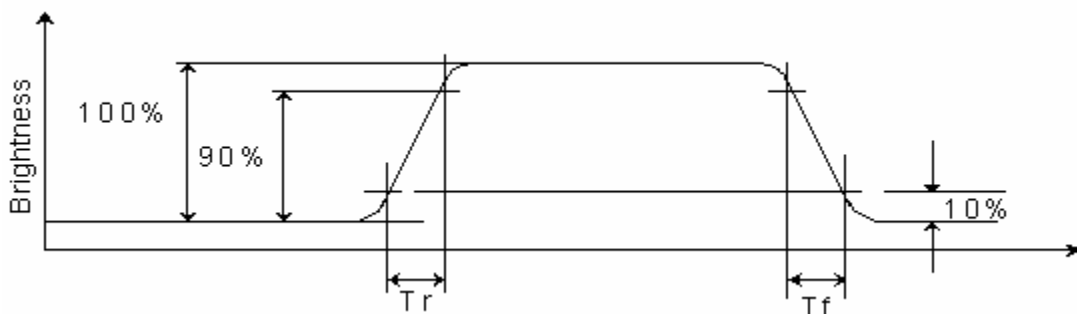

Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.
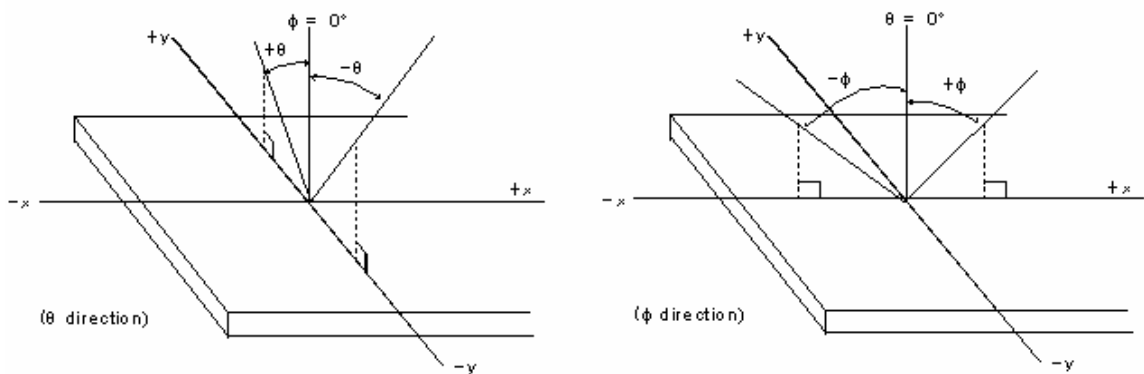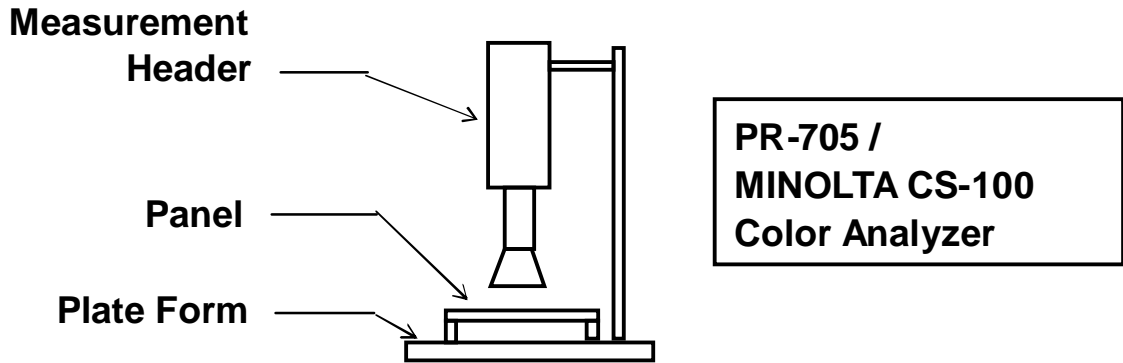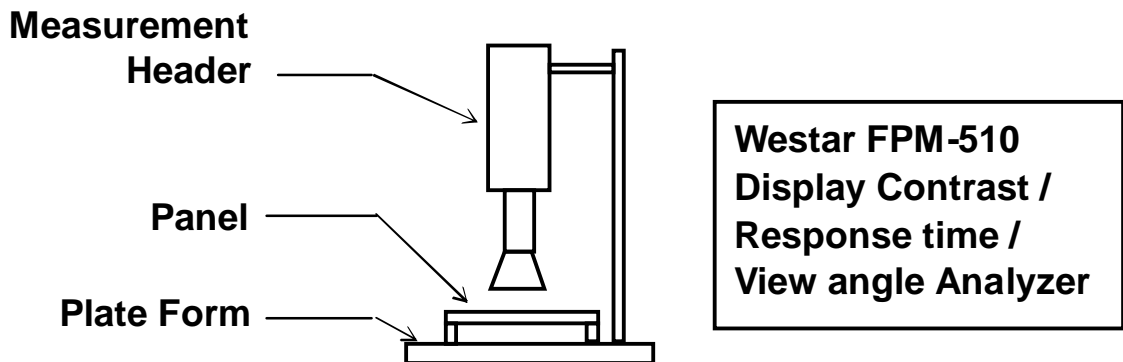

Figure 3: Viewing Angle

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APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

Measurement
Header

Panel

Plate Form

PR-705 /
MINOLTA CS-100
Color Analyzer

B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510

Measurement
Header

Panel

Plate Form

Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer

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C. ESD ON AIR DISCHARGE MODE
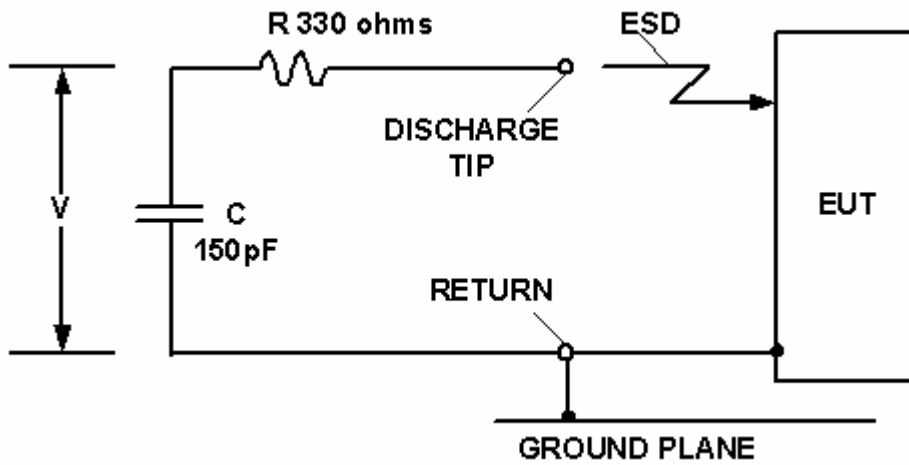
APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.